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QUESTION BANK (DESCRIPTIVE)

Subject with Code: Digital Logic Design (20CS0503)
Course & Branch: B.Tech –CSE, CSM, CAD, CCC, CIC, CSIT, CAI
Year &Sem: I-B.Tech& II-Sem **Regulation:** R20

UNIT –I
BINARY SYSTEMS & BOOLEAN ALGEBRA

1	a) Convert the following: i) $(41.6875)_{10}$to Hexadecimal number ii) $(11001101.0101)_2$to base-8 andbase-4	[L5] [CO1]	**6M**
	b) Using 2'scomplement, subtract $(111001)_2$ from $(101011)_2$.	[L5] [CO1]	**6M**
2	a) Convert the following numbers: i) $(AB)_{16}$=( )$_2$ ii) $(1234)_8$=( )$_{16}$	[L5] [CO1]	**4M**
	b) Convert $(AB33)_{16}$ to binary and then to gray code.	[L5] [CO1]	**4M**
	c) Using BCD arithmetic, perform addition of $(7129)_{10}$ + $(7711)_{10}$	[L5] [CO1]	**4M**
3	Convert the following: a) $(1AD)_{16}$=( )$_{10}$ b) $(453)_8$=( )$_{10}$ c) $(10110011)_2$=( )$_{10}$ d) $(5436)_{10}$=()$_{16}$	[L6] [CO1]	**12M**
4	Explain about complements with examples.	[L2] [CO1]	**12M**
5	a) Explain any Binary codes with examples.	[L2] [CO1]	**6M**
	b) Describe binary storage and registers.	[L2] [CO1]	**6M**
6	Prove the following identities: (i) A' B' C' + A' B C' + A B' C' + A B C' = C' (ii) A B + A B C + A' B + A B' C = B + A C	[L5] [CO1]	**6M**
	Reduce the following Boolean Expressions:		
7	a) A'C'+ABC+AC'+AB to three literals.	[L6] [CO1]	**4M**
	b) (X'Y'+Z)'+Z+XY+WZ to three literals.	[L6] [CO1]	**4M**
	c) A'B (D'+C'D) +B (A+A'CD) to one literal.	[L6] [CO1]	**4M**
8	a) Simplify the Boolean expressions to minimum number of literals. i) X' + XY + X Z'+XYZ' ii) (X+Y) (X+Y')	[L6] [CO1]	**6M**
	b) Obtain Complement of the following Boolean Expressions: i) A+B+A'B'C ii) AB + A (B +C) +B'(B+D)	[L5] [CO1]	**6M**
9	a) Express the Boolean function, F=A+B'C in sum of min terms form.	[L1] [CO1]	**6M**
	b) Convert Y=A(A+B+C) to standard POS form.	[L6] [CO1]	**6M**
10	a) Illustrate the digital logic gates with graphical symbol, algebraic function and truth table.	[L2] [CO1]	**8M**
	b) Define positive logic AND gate and negative logic OR gate.	[L1] [CO3]	**4M**

UNIT –II

GATE LEVEL MINIMIZATION

1	a) What is Karnaugh-Map? Explain four variable Karnaugh- Map. b) Simplify the given Boolean function using K-MAP and Implement using NAND gates. F(W, X,Y,Z)=XYZ+WXY+WYZ+WXZ	[L1] [CO1] [L6] [CO1]	**6M** **6M**
2	Reduce the function, f(x,y,z,w)= πM(0,2,4,5,6,7,8,10,13,15) using K-Map and draw the AOI logic diagram.	[L6] [CO5]	**12M**
3	Simplify the Boolean expression using K-MAP and draw the AOI logic diagram. F(A, B,C,D,E)=∑m(0,2,4,6,9,13,21,23,25,27,29,31)	[L6] [CO1]	**12M**
4	Simplify the given Boolean function using K-MAP and draw the logic diagram. F (A, B, C,D) = πM (3,5,6,7,11,13,14,15) and d(9,10,12)	[L6] [CO5]	**12M**
5	Simplify the Boolean function using K-MAP and draw the logic diagram. F (A, B,C,D) =∑m(1,2,3,8,9,10,11,14) + d(7,15)	[L6] [CO5]	**12M**
6	a) Why NAND and NOR gates are called Universal gates? and Implement F=AB+CD using two level implementation. b) Implement the function F = X′Y+X Y′+ Z using two level NAND implementation.	[L6] [CO1] [L6] [CO1]	**6M** **6M**
7	Simplify the given Boolean expression using K-map and implement using NAND gates. F(A,B,C,D)= ∑m(0,2,3,8,10,11,12,14)	[L6] [CO6]	**12M**
8	Simplify the following expressions, and implement them with two-level NAND gate circuits: a) AB′ + ABD + ABD′ + A′C′D′ + A′BC′ b) BD + BCD′ + AB′C′D′	[L6] [CO5] [L6] [CO5]	**6M** **6M**
9	a) Design the circuit using NAND gates for the given function. F= ABC'+DE+AB'D' b) For the given function, design the circuit using NOR gates. F= (X+Y). (X'+Y'+Z')	[L6] [CO5] [L6] [CO5]	**6M** **6M**
10	a) Implement EX-OR function with only NAND gates and AND-OR-NOT gates. b) Explain multilevel NAND circuits with an example.	[L6] [CO1] [L6] [CO1]	**6M** **6M**

UNIT –III

COMBINATIONAL LOGIC

1	a) Define combinational circuit and explain its analysis procedure.	[L1] [CO1]	**6M**
	b) Explain the procedure for designing a combinational circuit.	[L2] [CO2]	**6M**
2	a) Explain about Binary Half Adder with truth table and logic diagram.	[L2] [CO2]	**6M**
	b) Design and draw a full adder circuit.	[L3] [CO5]	**6M**
3	a) Design a 4-bit adder-subtractor circuit and explain its operation.	[L5] [CO2]	**6M**
	b) Explain about Decimal Adder with a neat diagram.	[L2] [CO1]	**6M**
4	a) Explain the working of a Carry- Look ahead adder.	[L2] [CO2]	**6M**
	b) Sketch BCD adder block diagram and explain its working.	[L3] [CO2]	**6M**
5	a) Design the combinational circuit of Binary to Excess-3 code convertor.	[L5] [CO2]	**6M**
	b) Design and implement 2-bit by 2-bit binary multiplier.	[L6] [CO2]	**6M**
6	a) What is a Magnitude comparator?	[L1] [CO1]	**4M**
	b) Design and implement a 2-bit Magnitude comparator.	[L3] [CO3]	**8M**
7	a) What is a Decoder? List its advantages.	[L1] [CO1]	**6M**
	b) Implement Full Adder using a Decoder and an OR gate.	[L5] [CO5]	**6M**
8	a) What is encoder? Design octal to binary encoder.	[L3] [CO5]	**6M**
	b) Explain in detail about Priority Encoder.	[L2] [CO4]	**6M**
9	a) Design and implement the following Boolean function by 8:1 Multiplexer. $(A,B,C.D)=\Sigma m(0,1,2,5,7,8,9,14,15)$.	[L3] [CO5]	**6M**
	b) Implement the following Boolean function by 8:1 multiplexer. F(A, B, C, D) = A'BD' + ACD + A'C' D +B'CD	[L5] [CO5]	**6M**
10	a) Design and implement a full subtractor using demultiplexer.	[L3] [CO6]	**6M**
	b) Design 1:8 demultiplexer using two 1:4 demultiplexer.	[L3] [CO4]	**6M**

Unit – IV
Synchronous Sequential Logic

1	a) Define a sequential circuit and draw its block diagram.	[L1] [CO1]	**4M**
	b) Differentiate between Combinational & Sequential circuits.	[L4] [CO4]	**4M**
	c) Distinguish between latches and flipflops.	[L2] [CO4]	**4M**
2	a) Explain the working principle of SR and JK flip-flops. Also give their characteristic table.	[L2] [CO3]	**6M**
	b) Explain the working principle of T and D flip-flops. Also give their characteristic table.	[L2] [CO3]	**6M**
3	a) Explain the analysis procedure of sequential circuits.	[L2] [CO4]	**4M**
	b) What is race-around condition? How race around condition is eliminated in a Master–slave J-K flip-flop?	[L2] [CO5]	**8M**
4	a) List the advantages and disadvantages of Flipflops.	[L1] [CO6]	**4M**
	b) What is the difference between Characteristic table and Excitation table? Give the excitation tables of SR, JK, T and D Flip flops.	[L2] [CO3]	**8M**
5	What is state diagram? Derive the simplified sequential circuit for the following state table.	[L3] [CO2]	**12M**

PS	Next State		Output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

6	a) What are the steps involved in design of a Synchronous Sequential circuit?	[L2] [CO1]	**5M**
	b) Define a Register. Explain in detail about various Shift Registers.	[L2] [CO4]	**7M**
7	a) What is a counter? List the applications of counters.	[L1] [CO6]	**4M**
	b) Explain in detail about 3-bit ripple Up-counter using suitable diagram.	[L2] [CO1]	**8M**
8	a) What is a synchronous counter? Draw the Block Diagram of 2-bit UP Counter.	[L1] [CO4]	**4M**
	b) Design and implement Mod-6 synchronous Counter using clocked T-flipflop.	[L5] [CO5]	**8M**
9	a) Differentiate synchronous and asynchronous counters.	[L4] [CO4]	**4M**
	b) Design a 3-bit Synchronous UP/DOWN Counter.	[L3] [CO5]	**8M**
10	a) Explain in detail about Ring counter and list its applications.	[L2] [CO3]	**6M**
	b) Explain in detail about Johnson counter and list its applications.	[L2] [CO3]	**6M**

Unit –V
Memory and Programmable Logic

1	a) What is RAM? Design a 4 X 4 RAM.	[L1] [CO1]	**8M**
	b) Explain in brief about memory decoding.	[L2] [CO1]	**4M**
2	a) What is an Error in digital systems? List the sources of errors.	L1] [CO4]	**4M**
	b) Explain about Error correction & Detection Codes with examples.	[L2] [CO1]	**8M**
3	a) Define and distinguish between PROM, PLA & PAL.	[L4] [CO4]	**6M**
	b) Design and implement the following Boolean expressions using PROM. F1(A, B, C) =Σm(0,2,4,7), F2(A,B,C)=Σm(1,3,5,7).	[L5] [CO6]	**6M**
4	a) Compare RAM and ROM.	[L2] [CO4]	**6M**
	b) List different types of ROMs.	[L1] [CO2]	**6M**
5	a) What is ROM? Explain combination of PLD's.	[L1] [CO4]	**6M**
	b) Design internal logic of a 32 x 8 ROM.	[L6] [CO4]	**6M**
6	a) What is PLA? List its applications.	[L1] [CO1]	**4M**
	b) Design and implement the following Boolean function using PLA. F1(A,B,C)=Σm(0,1,3,5) and F2(A,B,C)=Σm(0,3,5,7).	[L6] [CO6]	**8 M**
7	Design and implement the following functions using PLA. A(x,y,z)=∑m(1,2,4,6), B(x,y,z)=∑m(0,1,6,7), C(x,y,z)=∑m(2,6).	[L6] [CO6]	**12M**
8	a) What is PAL? List its applications.	[L1] [CO1]	**4M**
	b) Design and implement the following functions using PAL i) A(w,x,y,z) = Σm(0,2,6,7,8,9,12,13) ii) B(w,x,y,z)) = Σm(0,2,6,7,8,9,12,13,14)	[L6] [CO6]	**8M**
9	a) Explain in brief about Sequential programmable logic devices.	[L2] [CO4]	**8M**
	b) Explain basic Macrocell logic.	[L2] [CO5]	**4M**
10	a) Discuss about Complex programmable logic device.	[L2] [CO5]	**8M**
	b) What are Integrated Circuits? List its applications.	[L1] [CO1]	**4M**